

31011 U.S. PAT. 10/050348

01/15/02

JP

PATENT NUMBER and
ISSUE DATE

U.S. UTILITY Patent Application

100
1106

APPL. NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10050348	01/15/2002	438	438	2813	SCHILLINGEN

**APPLICANTS: Sandhu Gurtej; Moor John; Rueger Neal;

See

**CONTINUING DATA VERIFIED:

THIS APPLICATION IS A DIV OF 09/633,556 08/07/2000

See

ABANDONED

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**FOREIGN APPLICATIONS VERIFIED:

See

PG-PUB DO NOT PUBLISH <input type="checkbox"/>	RESCIND <input type="checkbox"/>
Foreign priority claimed: <input type="checkbox"/> yes <input type="checkbox"/> no	ATTORNEY DOCKET NO.
35 USC 119 conditions met: <input type="checkbox"/> yes <input type="checkbox"/> no	MI22-1898
Verified and Acknowledged Examiner's Initials	
TITLE: Transistor structures	

U.S. DEPT. OF COMM./PAT. & TM-PTO-436L (Rev. 12-94)

NOTICE OF ALLOWANCE MAILED

04/06/04

Assistant Examiner

Total Claims 3 Print Claim for O.G. 1

Amount Due	Date Paid
\$ 1630	

Primary Examiner

DRAWING		
Sheets Drwg.	Figs. Drwg.	Print Fig.
3	6	6

☐ TERMINAL
DISCLAIMER

PREPARED FOR ISSUE

Application Examiner 4/7/04

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